QUARTERLY REPORT NO. 11
FOR
ANALOG-TO-DIGITAL CONVERTER
CONTRACT NO. N00014-87-C-0314
1 October 1990—31 December 1990

ARPA Order Number:	9117
Program Code Number:	7220
Amount of Contract:	$3,152,507
Name of Contractor:	Texas Instruments Incorporated 13500 N. Central Expressway P.O. Box 655936, M.S. 105 Dallas, Texas 75265
Effective Date of Contract:	30 March 1987
Contract Expiration Date:	31 July 1991
Contract Number:	N00014-87-C-0314
Program Manager:	W.R. Wisseman (214) 995-2451
Principal Investigator:	Frank Morris (214) 995-6392
Short Title of Work:	GaAs A-to-D Converter
Contract Period Covered by Report:	1 October 1990—31 December 1990

16 January 1991

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I SUMMARY

A. Brief Program Definition

This is a research and development program to design and fabricate both a GaAs high sampling rate A/D converter (ADC) and a high-resolution GaAs ADC.

B. ADC Program Overview

We presented a joint paper entitled "A 1.2 Gsps 5-Bit Quantizer Fabricated With AlGaAs/GaAs Heterojunction Bipolar Transistors" at the 1990 GOMAC conference.

Work is under way to fabricate p-channel JFETs for characterization. The p-channel JFET will be used in the 12-bit ADC design instead of the n-channel JFET originally planned because the n-channel threshold voltage cannot be controlled with our present process.

Initial reliability data for the overgrowth HBTs looks impressive compared to recently reported results by TRW[1] and NTT.[2] Effort is continuing on the design and layout of the 12-bit ADC for a scheduled release in April 1991.

II. PROCESS DEVELOPMENT

Two lots of material are being processed with p-channel JFETs from the original GaAs ADC mask set, which used the $7 \times 7\ \mu m^2$ emitter HBTs and included both 4-bit and 5-bit quantizers. This mask set is being used since p-channel JFETs had already been included in some of the test circuits and the 1.5-μm channel length p-channel JFET required for the 12-bit ADC could be obtained by changing only one mask. The lots will not complete the entire ADC process but will include only those steps, through overgrowth, that will ensure that the resulting p-channel JFETs are compatible with our current ADC overgrowth process. The resulting p-channel JFETs will be available for dc characterization during January 1991. However, the ac characterization will represent only the

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[1] M.E. Hafizi et al., "Reliability Analysis of GaAs/AlGaAs HBTs Under Forward Current/Temperature Stress," *GaAs IC Symp.*, pp. 329-332 (1990).

[2] O. Nakajima et al., "Current-Induced Degradation of Be-Doped AlGaAs/GaAs HBTs and Its Suppression by Zn Diffusion Into Extrinsic Base Layer," *IEDM*, pp. 673-676 (1990).

worst case results, since the parasitic capacitances for these devices, originally designed with 5-μm channel lengths, will be significantly greater than for a "ground-up" 1.5-μm JFET design.

In addition to the two p-channel JFET lots described, a third lot has been started and will be stopped just before the channel threshold implant step. As soon as threshold data are available from the first two lots, the threshold implant will be tailored to give the desired threshold voltage.

A. ADC Process Transfer

Current-induced degradation of the I-V characteristics in AlGaAs/GaAs HBTs was reported by TRW and NTT for mesa HBTs with the base doped with beryllium. Similar degradation has been obtained by TI for their microwave mesa HBTs doped with zinc. Because of these results, TI has undertaken, with IR&D funding, a study of any potential degradation of the ADC overgrowth HBTs. HBTs from our most recent pilot line lot (Lot 104), which exhibited the 45 percent yield wafer, were packaged and placed on stress test. To accelerate the potential degradation process, our standard $5 \times 5\ \mu m^2$ emitter HBT was operated at 6 mA, which is 6× the design current used in both the 5-bit ADC and the 12-bit ADC. In addition, two other HBTs designed for output drivers with two and four ($5 \times 10\ \mu m^2$) emitter fingers were also stressed. The HBTs were biased with a constant V_{be} and V_{ce} and allowed to operate at the test current. After 1-week operation, the collector current was measured and compared to the original starting current. The ambient temperature was then increased to 55°C with the same bias conditions. After 1 week, the HBTs were cooled to room temperature and the collector current remeasured. This procedure continued with the temperature increased by an additional 25°C after each additional week of stress. After completion of the 230°C bias stress, the collector current had decreased approximately 3 percent for the $5 \times 5\ \mu m^2$ emitter HBTs. The two-finger emitter HBTs, which were stressed with 20-mA collector current, showned about a 2 to 3 percent increase in collector current; the four-finger emitter HBTs, stressed at 40 mA, showed no change after the 230°C stress. These HBTs have been operating for over 90 hours at 250°C and continue to be stable. These ADC results are consistent with our IR&D study on microwave mesa HBTs, which showed that, for base doping less than mid-$10^{18}/cm^3$ (as is the case for the ADC process), essentially no degradation with current stress is detected.

Two remaining 5-bit ADC pilot line lots are in process with completion expected in January 1991 and March 1991. The second lot (SWR 265) is an experimental ADC lot of six carbon-doped base wafers from Kopin. Also included in this lot are five zinc-doped wafers from TI's new epitaxy facility. Highly doped InGaAs cap layers have been grown on some wafers of this lot for improved emitter ohmic contacts.

B. Circuit Design/Testing

Our joint paper entitled "A 1.2 Gsps 5-Bit Quantizer Fabricated With AlGaAs/GaAs Heterojunction Bipolar Transistors" was presented by Hughes at the 1990 GOMAC conference. This work was performed under Contract No. N00014-87-C-0314 to develop GaAs HBT ADCs.

At the request of Texas Instruments, Hughes evaluated the applicability of a 1.5-μm gate-length p-channel JFET to the 12-bit ADC design. Comparison between the n-channel and p-channel parasitics (Table 1) reveals that the p-channel device parasitics are a factor of 15 larger than the n-channel parameters. This capacitance increase results in reduced ADC speed/power performance. A brief evaluation was performed by modifying the sample-and-hold (S/H) circuits to use p-channel devices in place of the baseline n-channel devices and running a core set of circuit simulations. Linearity, distortion, acquisition, and settling simulations indicate that the p-channel model will just meet a 20-MHz sample rate. However, several critical p-channel device parameters, based on projected expectations, must be measured to ensure this device will be adequate for the 12-bit design. These parameters include drain-to-source breakdown voltage ($BV_{ds} > 8$ V), early voltage (>50 V), and 1/f noise corner frequency (< 200 kHz).

Table 1. n-Channel Versus p-Channel JFET Device Parameters

Parameter	n-Channel	p-Channel
Gate length, minimum (μm)	3	1.5
Gate width (μm) for I_{ds} = 1 mA	3.5	60
C_{gs} (fF)	30	550
C_{gd} (fF)	6	90

Because of processing problems encountered with the n-channel JFET, the p-channel device will become our baseline high-impedance load device for the 12-bit ADC design. Since every amplifier design in the 12-bit ADC must be modified and resimulated with the p-channel devices, the targeted 12-bit ADC release date is 1 April 1991.

We continued to make progress throughout the quarter in design and layout capture of the 12-bit ADC. To ensure an error-free design, we are preparing the 12-bit ADC for computer-automated hierarchical layout versus schematic (LVS) checking. The LVS tool verifies that the schematic representation of the circuit used for simulation purposes matches the cell layout in both interconnect and component selection. This procedure will significantly reduce the possibility of a layout error in the 12-bit ADC. Toward this goal, all the 12-bit ADC schematics have been formatted for LVS.

III. PERSONNEL ASSIGNMENTS

There have been no changes in personnel.

IV. PLANS

- TI will:
  - Continue to improve n-ohmic metal process.
  - CRL will continue interfacing with the Pilot Line to ensure smooth process transfer.
  - Pilot Line will continue processing the lots in progress.
- Hughes will:
  - Complete design and layout of the monolithic 12-bit ADC.

V. UNOFFICIAL DARPA FINANCIAL STATUS REPORT

This is the financial status as of 31December 1990:

Funds Authorized	Funds Spent	Amount Billed	Amount Received
$2,978,246	$2,928,246	$2,651,734	$2,636,735

Contract Number: N00014-87-C-0314

Contract Title: GaAs Heterojunction Device-Based A/D

Start Date: 30 March 1987

F.J. MORRIS, Principal Investigator
System Components Laboratory

H.T. YUAN, Manager
GaAs Logic and Memory Branch

W.R. WISSEMAN, Program Manager
System Components Laboratory